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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,178	03/17/2004	Yasunori Kurosawa	81754.0114	4143
26021	7590	02/07/2006	EXAMINER	
HOGAN & HARTSON L.L.P. 500 S. GRAND AVENUE SUITE 1900 LOS ANGELES, CA 90071-2611			DOAN, THERESA T	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/803,178	Applicant(s) KUROSAWA ET AL.	
	Examiner Theresa T. Doan	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 January 2006.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2,3,10 and 11 is/are allowed.
- 6) ☒ Claim(s) 1, 4-9 and 12-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>01/03/06</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The prior art documents submitted by applicant in the Information Disclosure Statement filed on 01/03/06, have all been considered and made of record (note the attached copy of form PTO-1449).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4-6, 9 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (U.S. Pat. 6,455,408) in view of Hsuan et al. (U.S. Pat. 6,166,444) as previously cited.

Regarding claims 1 and 9, Hwang (Figs. 15-17) discloses a semiconductor device or wafer 50 (column 3, lines 52-53), comprising: a semiconductor substrate 52 (column 3, lines 55-56) provided with a plurality of integrated circuits (not shown, see column 3, lines 54-56) and pads 54; a semiconductor chip 90 of the semiconductor wafer 50 provided with an integrated circuits (not shown, see column 3, lines 54-56) and a pad 54 (Fig. 17); a wiring layer (64,70) that has a concave portion 68 (column 4, lines 60-65) and is electrically connected to the pad 54; an external terminal (78,80) that is

joined directly to the concave portion 68 of the wiring layer (64,70) without any intervening layers (see Figs. 16-17 Labeled by the examiner below and column 5, lines 61-63); and a polyimide or epoxy resin layer 74 (column 5, lines 30-38 and column 3, lines 66-67 through column 4, lines 1-2) provided with a through hole and disposed on the wiring layer 64, the through hole and the concave portion 68 residing at the same position (see Fig. 16 below and column 5, lines 28-30).

Hwang discloses a semiconductor chip 90 provided with the integrated circuit and a pad 54, but does not specifically disclose that the pad 54 is electrically connected to the integrated circuit.

However, Hsuan (Fig. 3) teaches a semiconductor chip 30 provided with an integrated circuit 32 and a pad 42 (column 3, lines 19-20), the pad 42 is electrically connected to the integrated circuit 32 (column 3, lines 15-17) and to the external terminals 56. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide the semiconductor chip of Hwang with the pad 54 electrically connected to the integrated circuit in order to provide the electrically connects between the integrated circuit and the external terminals, as taught by Hsuan (see Fig. 3).

FIG. 16

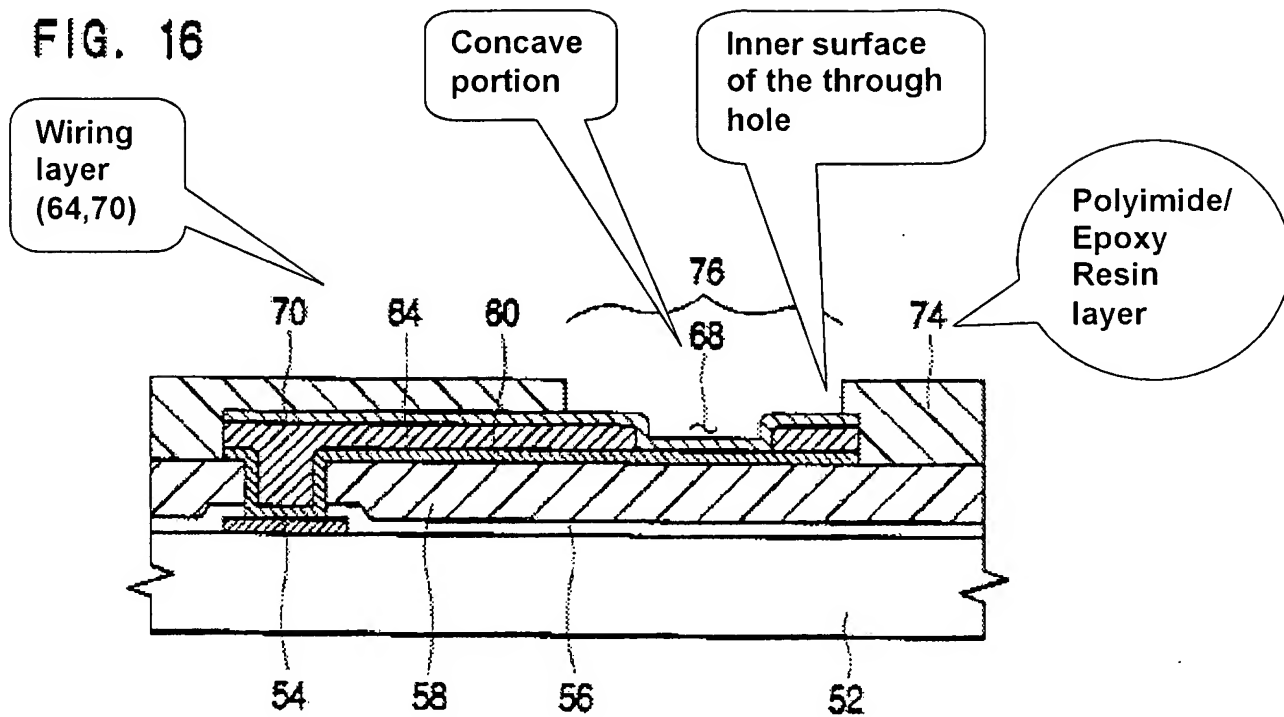
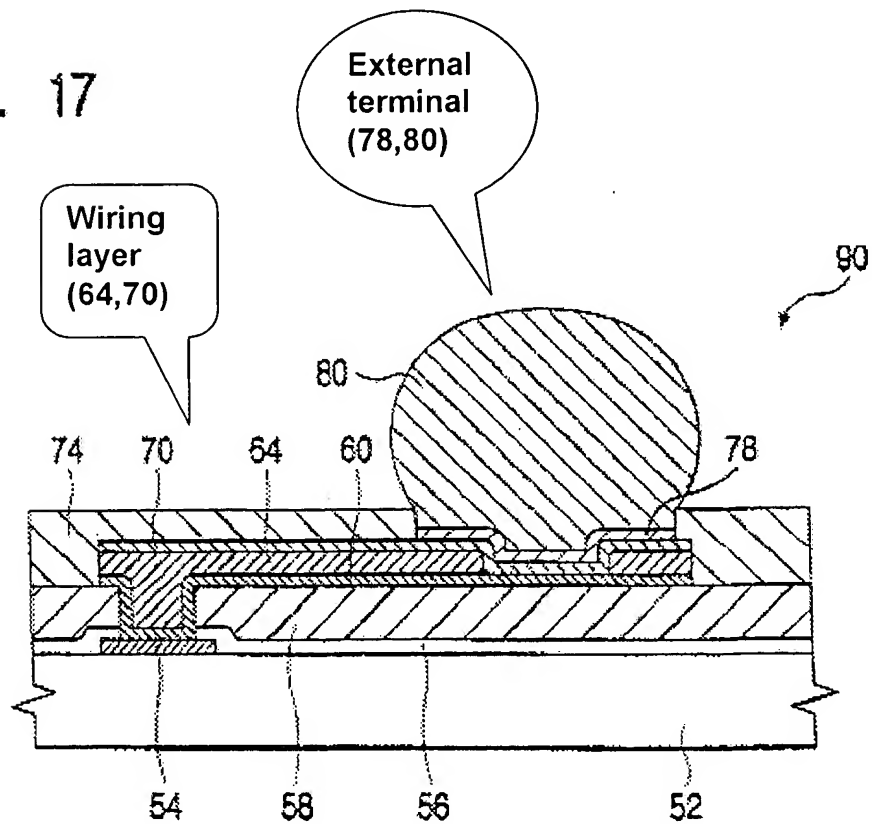


FIG. 17



Regarding claims 4 and 12, Hwang discloses that an inner surface of the through hole in the resin layer 74 is in contact with the external terminal (78,80) (see Fig. 17 Labeled by the examiner above).

Regarding claims 5 and 13, Hwang (Fig. 17) further discloses a stress relaxation layer 58 (column 3, lines 66-67 through column 4, lines 1-2) disposed on the semiconductor chip 50, wherein the wiring layer (64,70) is disposed on the stress relaxation layer 58.

Regarding claims 6 and 14, Hwang discloses that the resin layer 74 is prepared from a solder resist of polyimide (column 5, lines 28-37).

4. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (U.S. Pat. 6,455,408) in view of Hsuan et al. (U.S. Pat. 6,166,444) as applied to claim 1 above, and further in view of Farnworth et al. (U.S. Pat. 6,767,817) as previously cited.

Regarding claim 7, Hwang does not disclose that a circuit board comprising the semiconductor chip 90 disclosed in Fig. 17.

However, Farnworth (Fig. 2) teaches an integrated circuit package 36 (column 4, lines 1-3) including a circuit board 54 comprising a semiconductor chip 40 (column 4, lines 14-17). Accordingly, it would have been obvious to one having ordinary skill in the

art at the time of the invention was made to provide a circuit board comprising the semiconductor chip 90 of Hwang in order to form an integrated circuit package which is used in the desired electronic applications, as taught by Farnworth (column 4, lines 1-5).

Regarding claim 8, Hwang does not disclose that an electronic apparatus comprising the semiconductor chip 90 disclosed in Fig. 17.

However, Farnworth (Fig. 1) also teaches an electronic apparatus system 10 comprising an integrated circuit package 36 including a semiconductor chip 40 (Fig. 2 and column 4, lines 1-5). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide an electronic apparatus comprising the semiconductor chip 90 of Hwang in order to form a desired electronic application such as a computer, audio or visual device, as taught by Farnworth (column 3, lines 15-21).

Allowable Subject Matter

5. Claims 2-3 and 10-11 are allowed (see reasons of record).

Response to Arguments

6. The double patenting of the last office action is overcome by the Terminal Disclaimer that filed on 01/03/06.

7. Applicant argues that the combination of Hwang, Hsuan and Farnworth is not disclosed the limitations of the amendment claims 1 and 9.

This argument is not persuasive because Hwang (Figs. 16-17 labeled by the examiner above) discloses a wiring layer (64,70) that has a concave portion 68 (column 4, lines 60-65) and an external terminal (78,80) that is joined directly to the concave portion 68 of the wiring layer (64,70) without any intervening layers (column 5, lines 61-63). Therefore, Hwang teaches all the limitations of the amendment claims 1 and 9.

The rest of applicant's arguments, addressed to the amended claims are considered in the rejections shown above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-

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1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
January 25, 2006.



PHAT X. CAO
PRIMARY EXAMINER